Junwei Huang

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Research Interests: Integrated voltage regulators (IVR); hybrid switched-capacitor/inductor DC-DC converters; high-conversion-ratio power delivery; fast transient response; vertical power delivery; scalable multi-module power systems; chiplet/Power Chiplet architectures

EDUCATION

2018.08–2024.07	University of Macau	Electrical and Computer Engineering	Ph.D. Advisors: Prof. Yan Lu and Prof. Chi-Seng Lam
2014.09–2018.06	University of Electronic Science and Technology of China	Microelectronics Science and Engineering	B.Eng.

ACADEMIC APPOINTMENTS

2025.09–present	University of California, Berkeley	Department of Electrical Engineering and Computer Sciences (EECS)	Visiting Postdoctoral Researcher Faculty Host: Prof. Robert Pilawa-Podgurski
2025.09–present	University of Macau	Institute of Microelectronics	Postdoctoral Fellow PI: Prof. Rui P. Martins and Prof. Sai-Weng Sin
2024.10–2025.09	University of Macau	Institute of Microelectronics	Research Assistant PI: Prof. Rui P. Martins
2024.11–2025.05	Tsinghua University	Department of Electronic Engineering	Visiting Scholar Faculty Host: Prof. Yan Lu

RESEARCH SUMMARY

University of California, Berkeley, EECS **2025.09–present**

- Research focuses on the co-design of board-level power electronics and on-interposer high-voltage integrated voltage regulators (HV-IVR, >6 V input) for next-generation GPU/CPU power delivery, leveraging hybrid switched-capacitor/inductor converter topologies and scalable distributed converter arrays to achieve high aggregate current, high current density, and high power density.

University of Macau, State Key Laboratory of Analog and Mixed-Signal VLSI **2018.08–2025.09**

- Designed and taped out multiple hybrid SC/inductor DC-DC converters in 65 nm CMOS and 180 nm BCD processes, covering the full IC design cycle from topology innovation, circuit/layout implementation, to silicon measurement.
- Demonstrated state-of-the-art efficiency (96.1% at 4-to-1.2 V), current density (1.46 A/mm2 at 12:1), and transient response (63 mV droop @ 3.5 A load step) across hybrid converters with conversion ratios from 4:1 to 12:1.
- Pioneered a scalable multi-module parallel architecture with one-pin decentralized current balancing, reducing interconnect complexity from O(N) to O(1) — directly applicable to IVR arrays and vertical power delivery.
- 25 publications: 1 ISSCC highlight paper (1st author), 3 CICC 1st-author, 2 JSSC 1st-author, 1 TCAS-I 1st-author. Total: 6 ISSCC + 6 JSSC contributions.

TECHNICAL SKILLS

- **IC Design:** Full-custom analog/mixed-signal IC design (schematic, layout, DRC/LVS, post-layout simulation, tape-out, lab measurement); switched-capacitor and hybrid DC-DC converter topologies; multi-loop control design; power stage optimization
- **Process Technologies:** 65 nm CMOS, 180 nm BCD (high-voltage NMOS/PMOS)
- **EDA Tools:** Cadence Virtuoso (Spectre, Layout XL), Ansys (HFSS/Maxwell), MATLAB/Simulink, Altium Designer (PCB)
- **Lab Equipment:** Oscilloscopes, spectrum analyzers, semiconductor parameter analyzers, probe stations; board-level power converter testing; multi-chip measurement and characterization
- **Programming:** SKILL (Cadence), Python, MATLAB, Verilog (digital control blocks)

AWARDS AND ACADEMIC SERVICE

1. Akrostar Technology Academic Prize for the academic year 2023/2024 (Top 3).
2. Reviewer for IEEE TIE, IEEE OJIE, IEEE TCAS-I, IEEE TCAS-II, IEEE OJCAS.
3. Invited presenter at IEEE PES/PELS event at UC Berkeley.

PUBLICATIONS

First-Author Conference Papers:

[C1] **J. Huang**, X. Mao, Z. Tong, Z. Yu, W. Yang, C.-S. Lam, R. P. Martins, Y. Lu, "A 20MHz-1MHz Dual-Loop Non-Uniform-Multi-Inductor Hybrid DC-DC Converter with Specified Inductor Current Allocation and Fast Transient Response," ISSCC 2025. *(Highlight Paper)* *[IVR-relevant: dual-loop control with non-uniform inductors achieving 63 mV droop @ 3.5 A load step and 91.4% peak efficiency in 180 nm BCD]*

[C2] **J. Huang**, Z. Tong, X. Mao, C.-S. Lam, R. P. Martins, Y. Lu, "A Fast-Slow Two-Module DC-DC Solution with Transient and Efficiency Improvements for 2.5D/3D Integration," CICC 2024.

[C3] **J. Huang**, Z. Tong, Y. Lu, C.-S. Lam, R. P. Martins, "A 5V-to-0.5V Inductor-First Inductor-on-Ground Switched Capacitor Multi-Path Hybrid DC-DC Converter," CICC 2023. *[IVR-relevant: inductor-first topology enabling continuous input current and 1.02 A/mm2 current density at up to 10:1 step-down, 96.1% peak efficiency]*

[C4] **J. Huang**, X. Mao, Z. Tong, Z. Yu, S. Han, C.-S. Lam, R. P. Martins, Y. Lu, "A Scalable Distributed 12-to-1V Fast-Slow Hybrid DC-DC Combo with Fast-Transient Bucklets and One-Pin Current Balancing," CICC 2026. *(Accepted)* *[IVR-relevant: scalable 4-phase array with one-pin decentralized current balancing, 22 A total output, 1.46 A/mm2, 55 mV droop @ 6 A/20 ns load step]*

First-Author Journal Papers:

[J1] **J. Huang**, Z. Tong, X. Mao, C.-S. Lam, R. P. Martins, Y. Lu, "A Fast-Slow Two-Module High-Power-Density DC-DC Solution With Transient and Efficiency Improvements," IEEE JSSC, 2025. *[Two-module fast-slow hybrid architecture for 2.5D/3D integration with improved transient and efficiency]*

[J2] **J. Huang**, Z. Tong, C.-S. Lam, X. Mao, R. P. Martins, Y. Lu, "A Multi-Path Inductor-First Inductor-on-Ground Switched-Capacitor Hybrid DC-DC Converter," IEEE JSSC, 2024. *[Inductor-first multi-path topology achieving 96.1% peak efficiency and 1.02 A/mm2 current density]*

[J3] **J. Huang**, C.-S. Lam, Y. Lu, R. P. Martins, "A Symmetrical Double Step-Down Converter with Extended Voltage Conversion Ratio," IEEE TCAS-I, 2022. *[Symmetrical topology extending voltage conversion ratio for step-down applications]*

Co-Authored Conference Papers:

[C5] Z. Tong, **J. Huang**, Y. Lu, R. P. Martins, "A 42W Reconfigurable Bidirectional Power Delivery Voltage-Regulating Cable," ISSCC 2023. *(Highlight Paper)*

[C6] Z. Zhu, **J. Huang**, Z. Song, Z. Yu, S. Han, S-W. Sin, Y. Lu, "An Inductor-at-Middle Hybrid Buck Converter with Shared Power-Signal Path for Distributed Vertical Power Delivery," ISSCC 2026.

[C7] Z. Yu, Z. Tong, **J. Huang**, J. Yin, Y. Lu, "A Compact Dual-Capacitor Relay SPT Supply Modulator with Overshoot-Free Adaptive On-Time Control for 5G FR2 CMOS PA," ISSCC 2026.

[C8] Z. Tong, Z. Yu, **J. Huang**, X. Mao, B. Wicht, R. P. Martins, Y. Lu, "HOOP: A Scalable Hybrid DC-DC Converter Ring for High Performance Computing," ISSCC 2025.

[C9] W. Yang, Z. Tong, **J. Huang**, R. P. Martins, Y. Lu, "A Bi-Directional Dual-Path Boost-48V-Buck Hybrid Converter for High-Voltage Power Transmission Cable in Light-Weight Humanoid Robots," ISSCC 2025.

[C10] Z. Yu, **J. Huang**, Z. Tong, Z. Zhu, Y. Lu, "An Output-Rail-Scalable Hybrid Buck Converter with Globally Adaptive Frequency Control Achieving 98.0% Peak Efficiency and 490 mW/mm3 Power Density," CICC 2026. *(Accepted)*

[C11] S. Han, **J. Huang**, F. Song, Z. Tong, S-W Sin, H. Jiang, X. Wu, T. Ren, Y. Lu, "A 94.1% Peak Efficiency Coupled-Inductor Boost Converter with Small Inductor Current Ripple and Fast Transient Response," CICC 2026. *(Accepted)*

[C12] Z. Song, Z. Tong, **J. Huang**, Z. Zhu, S-W Sin, Y. Lu, "A 6V-to-1V ReSC-Hybrid Two-Stage Merged Buck Converter with an Ultra-Small Inductor for VPD," CICC 2026. *(Accepted)*

[C13] X. Mao, **J. Huang**, Z. Tong, R. P. Martins, Y. Lu, "A Quad-Output Hybrid Buck Converter with 8-Inductor Helping One Spot from All Quarters for Multi-Core XPUs," CICC 2024.

[C14] Z. Tong, W. Yang, S. Han, **J. Huang**, X. Mao, Y. Lu, "Where is the Inductor: A Review and Comparison of the Hybrid DC-DC Buck Topologies," CICC 2025.

[C15] Z. Yu, **J. Huang**, Z. Tong, M. Huang, Y. Lu, "An Always Dual-Path Hybrid DC-DC Converter with Multiphase Interleaving Switched-Capacitor Cell Obtaining 45% Output Ripple Reduction," ISCAS 2025.

[C16] F. Luo, **J. Huang**, M. Huang, Y. Lu, "A 12V-Input 1.8V-0.8V-Output Multiple-Output Hybrid Buck DC-DC Converter with a Shared Flying Capacitor," ISCAS 2025.

[C17] Y. Hu, **J. Huang**, M. Huang, Y. Lu, "A 5V-to-0.8V Inductor-First 2L2C Multi-Path Hybrid DC-DC Converter," ISCAS 2025.

Co-Authored Journal Papers:

[J4] Z. Tong, **J. Huang**, X. Mao, R. P. Martins, Y. Lu, "A Double Pulse Overlapping Laser Diode Driver with Minimum 100-ps Pulse for LiDAR System," IEEE JSSC, 2024.

[J5] Z. Tong, **J. Huang**, X. Mao, R. P. Martins, Y. Lu, "A Bidirectional USB Power Delivery Voltage-Regulating Cable," IEEE JSSC, 2024.

[J6] W. Yang, Z. Tong, **J. Huang**, R. P. Martins, Y. Lu, "A Bi-Directional Dual-Path Boost-Buck Hybrid Converter for High-Voltage Power Transmission Delivery Cable in Humanoid Robots," IEEE JSSC, 2025.

[J7] Y. Lu, **J. Huang**, Z. Tong, T. Hu, W.-L. Zeng, M. Huang, X. Mao, G. Cai, "An Overview of Hybrid DC-DC Converters: From Seeds to Leaves," IEEE OJ-SSCS, 2024.

[J8] Y. Lu, G. Cai, **J. Huang**, "Favorable basic cells for hybrid DC-DC converters," J. Semiconductors, 2023.